



P-Channel Enhancement Mode Field Effect Transistor

● Features

$V_{DS} (V) = -20V, I_D = -2.5A$

$R_{DS(ON)} < 160m\Omega @ V_{GS} = -4.5V$

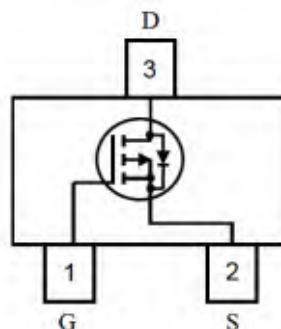
$R_{DS(ON)} < 230m\Omega @ V_{GS} = -2.5V$

SOT23 Package

● General Description

These P-Channel enhancement mode field effect transistors are produced using high cell density, DMOS technology.

● Pin Configurations



● Absolute Maximum Ratings @ $T_A=25^{\circ}C$ unless otherwise noted

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate-Source Voltage		V_{GSS}	± 8	V
Drain Current (Continuous)	$T_A=25^{\circ}C$	I_D	-2.5	A
	$T_A=70^{\circ}C$		-1.8	
Drain Current (Pulse)		I_{DM}	-8	A
Power Dissipation	$T_A=25^{\circ}C$	P_D	1	W
Operating Temperature/ Storage Temperature		T_J/T_{STG}	-55~150	$^{\circ}C$



ZLM0201AB

● Electrical Characteristics @T_A=25°C unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ON/OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20V, V_{GS} = 0V$	--	--	-1	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_{DS} = -250\mu A$	-0.5	-0.65	-1	V
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 8V, V_{DS} = 0V$	--	--	± 100	nA
Drain-Source On-state Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -1A$	--	120	160	m Ω
		$V_{GS} = -2.5V, I_D = -1A$	--	170	230	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = -5V, I_D = -3A$	--	8	--	S
Diode Forward Voltage	V_{SD}	$I_{SD} = -1.6A, V_{GS} = 0V$	--	--	-1.2	V
Switching CHARACTERISTICS						
Total Gate Charge	Q_g	$V_{DS} = -6V, I_D = -2.8A$ $V_{GS} = -4.5V$	--	5.4	--	nC
Gate-Source Charge	Q_{gs}		--	0.8	--	nC
Gate-Drain Charge	Q_{gd}		--	1.2	--	nC
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -6V, R_L = 6\Omega$ $I_D = -1A, V_{GEN} = -4.5V$ $R_G = 6\Omega$	--	11	--	ns
Turn-on Rise Time	t_r		--	25	--	ns
Turn-off Delay Time	$t_{d(off)}$		--	32	--	ns
Turn-off Fall Time	t_f		--	8.6	--	ns
Dynamic CHARACTERISTICS						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -6V, f = 1.0MHz$	--	405	--	pF
Output Capacitance	C_{oss}		--	78	--	pF
Reverse Transfer Capacitance	C_{rss}		--	65	--	pF

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test: $PW \leq 300\mu s$, duty cycle $\leq 2\%$.
3. For design AID only, not subject to production testing.
4. Switching time is essentially independent of operating temperature.



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

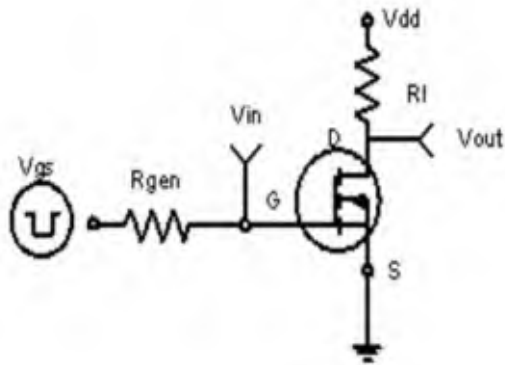


Figure 1: Switching Test Circuit

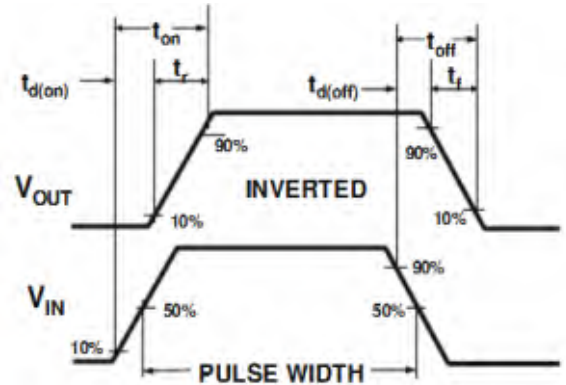


Figure 2: Switching Waveforms

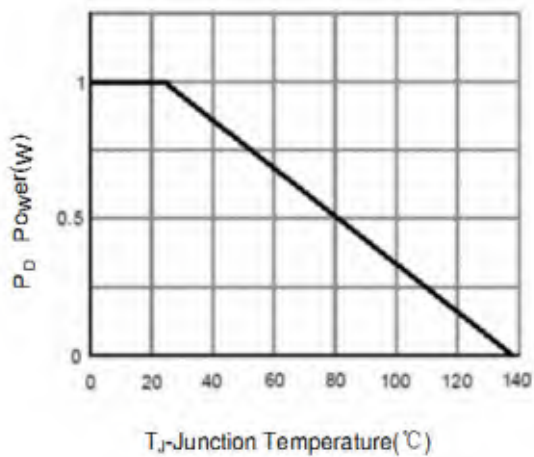


Figure 3 Power Dissipation

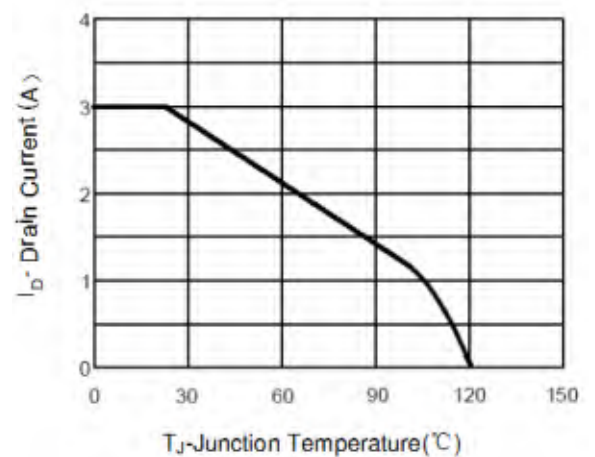


Figure 4 Drain Current

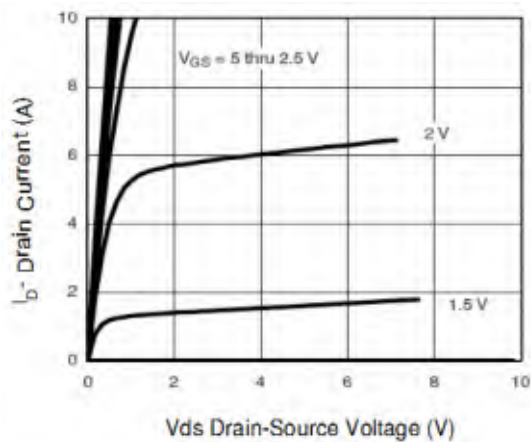


Figure 5 Output CHARACTERISTICS

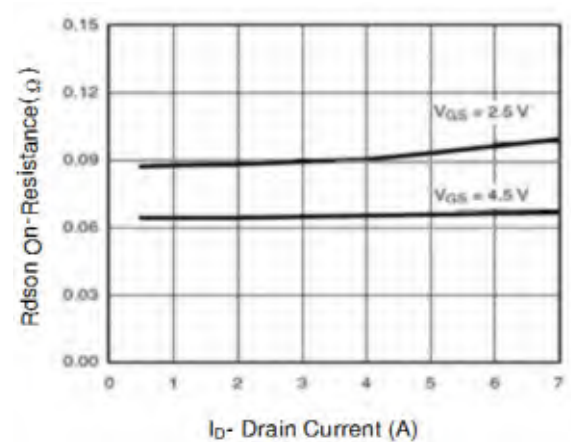


Figure 6 Drain-Source On-Resistance



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

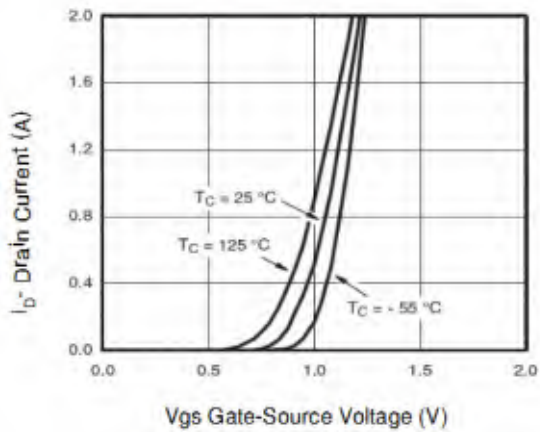


Figure 7 Transfer Characteristics

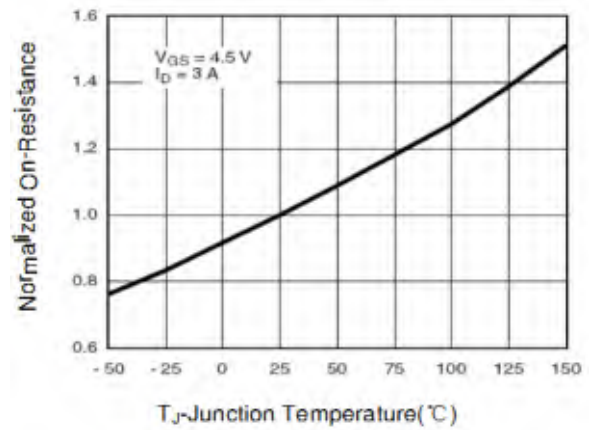


Figure 8 Drain-Source On-Resistance

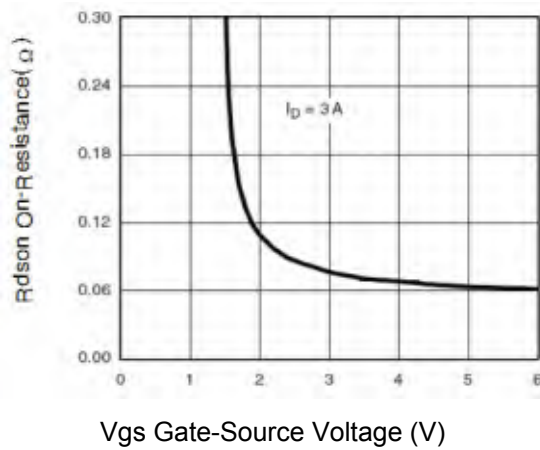


Figure 9 $R_{DS(on)}$ vs V_{GS}

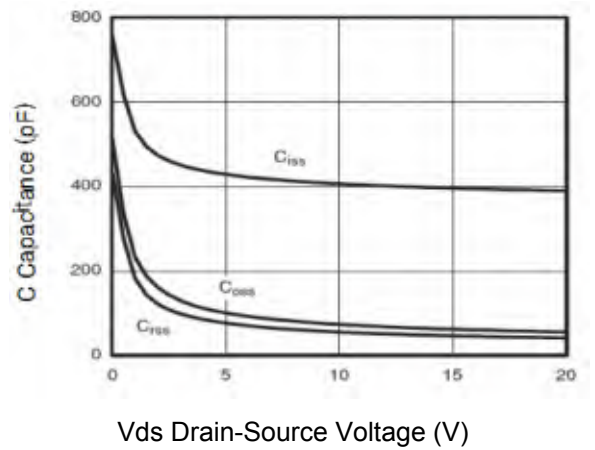


Figure 10 Capacitance vs V_{DS}

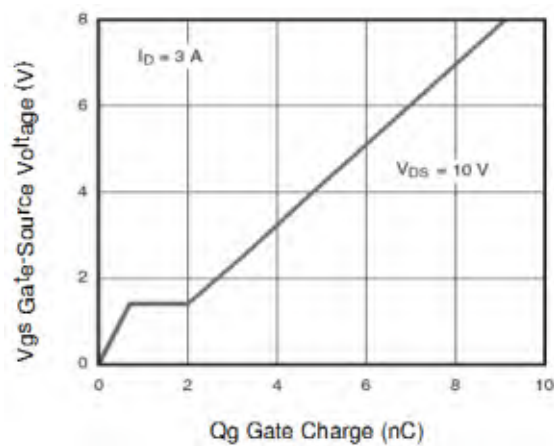


Figure 11 Gate Charge

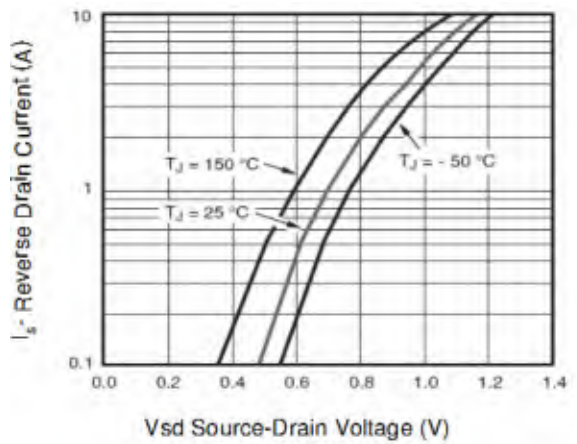
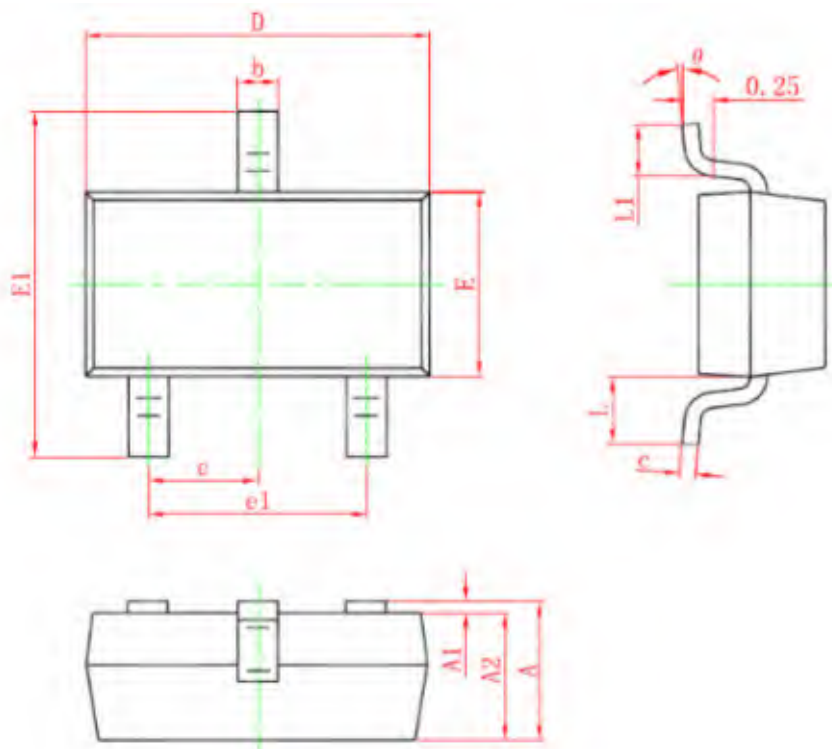


Figure 12 Source- Drain Diode Forward



● Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°