General Description

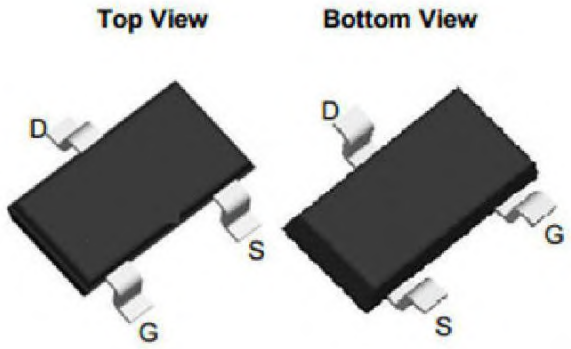
The ZLM0301AB uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

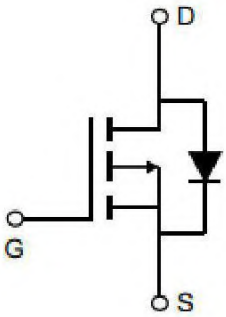
Applications

- Notebook
- Load Switch
- Battery Protection
- Hand-held Instruments
- USB cable

Product Summary

V_{DS}	-30V
I_D (at V_{GS} =10V)	-3.2A
$R_{DS(ON)}$ (at V_{GS} =-10V)	< 58mΩ
$R_{DS(ON)}$ (at V_{GS} =-4.5V)	< 60mΩ





Absolute MaximumRatings TA=25°Cunless otherwisenoted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±12	V
ContinuousDrain Current	TA=25°C	I_D	-3.2	A
	TA=70°C		-2.6	
PulsedDrainCurrent[A]		I_{DM}	-12.6	A
Power Dissipation	TA=25°C	P_D	0.9	W
	TA=70°C		0.5	
Storage Temperature Range		T_{STG}	-55 to +150	°C
Operating Junction Temperature Range		T_J	-55 to +150	°C
Thermal Resistance, Junction-to-Ambient		$R_{\theta JA}$	90	°C/W

Electrical Characteristics (TJ=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250uA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V,V_{GS}=0V			-1	uA
I_{GSS}	Gate-Bodyleakagecurrent	V_{DS}=0V,V_{GS}=±12V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250uA	-0.5	-0.9	-1.5	V
$I_{D(ON)}$	Onstate draincurrent	V_{GS}=10V,V_{DS}=5V	-12.6			A
$R_{DS(ON)}$	StaticDrain-Source On-Resistance	V_{GS}=-10V,I_D=-1A		38	58	mΩ
		V_{GS}=-4.5V,I_D=-1A		42	60	mΩ
g_{FS}	ForwardTransconductance	V_{DS}=-5V,I_D=-4.1A		7		S
V_{SD}	Diode Forward Voltage	I_{DS}=-1A,V_{GS}=0V		-0.7	-1.5	V
I_S	Maximum Body-Diode ContinuousCurrent				-3.7	A
DYNAMIC PARAMETERS						
C_{iss}	InputCapacitance	V_{GS}=0V,V_{DS}=-15V, f=1MHz		815		pF
C_{oss}	OutputCapacitance			60		pF
C_{rss}	Reverse TransferCapacitance			50		pF
SWITCHING PARAMETERS						
Q_g	TotalGate Charge[2,3]	V_{GS}=-4.5V,V_{DS}=-15V, I_D=-3.2A		7.8		nC
Q_{gs}	Gate Source Charge[2,3]			2.1		nC
Q_{gd}	Gate Drain Charge[2,3]			2.4		nC
$t_{D(on)}$	Turn-OnDelayTime[2,3]	V_{GS}=-10V,V_{DS}=-15V, R_G=3Ω,I_D=-4A		12.4		ns
t_r	Turn-On Rise Time[2,3]			5.6		ns
$t_{D(off)}$	Turn-OffDelayTime[2,3]			43.2		ns
t_f	Turn-OffFallTime[2,3]			6.8		ns

Notes:

A. is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference isdefined as the solder mounting surface of the drain pins.RθJC is guaranteed by design while $R_{\theta CA}$ is determined by theuser's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.

B.The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C.Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initialTJ=25°C.

D.The static characteristics in Figures 1 to 6 are obtained using <300 s pulses, duty cycle 0.5% max.

E.These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

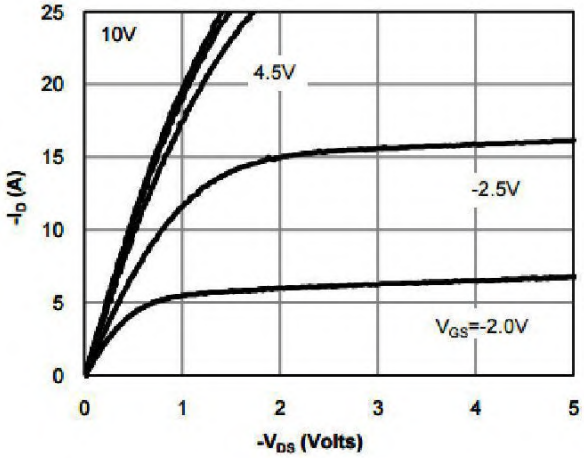


Fig 1: On-Region Characteristics (Note D)

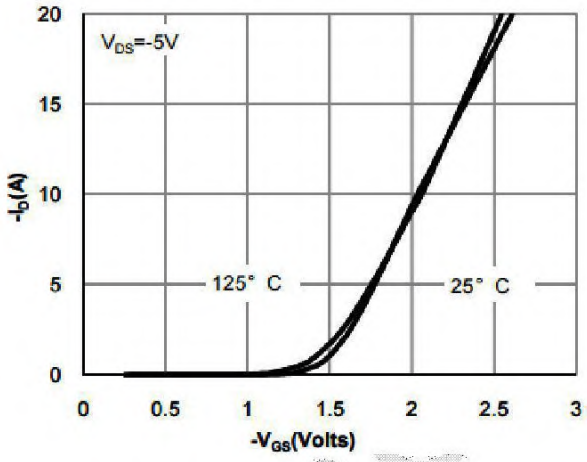


Figure 2: Transfer Characteristics (Note D)

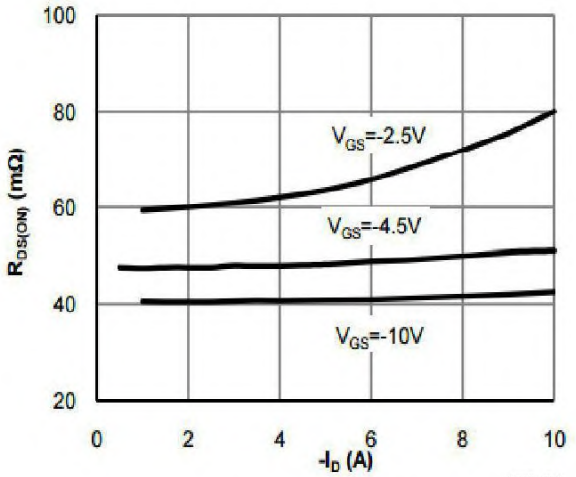


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note D)

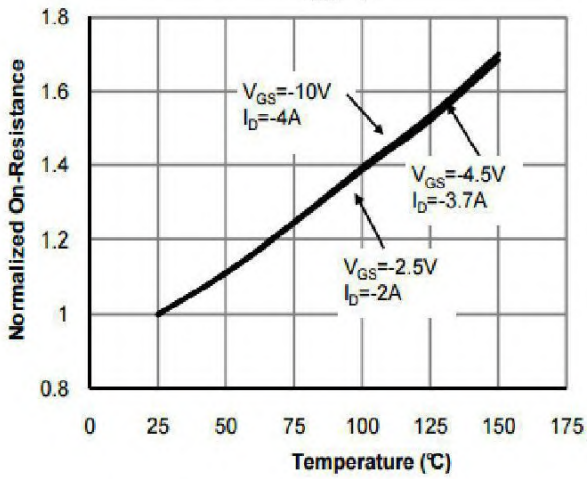


Figure 4: On-Resistance vs. Junction Temperature (Note D)

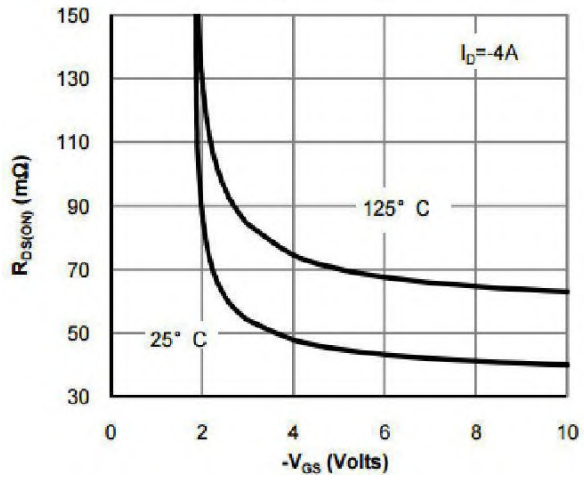


Figure 5: On-Resistance vs. Gate-Source Voltage (Note D)

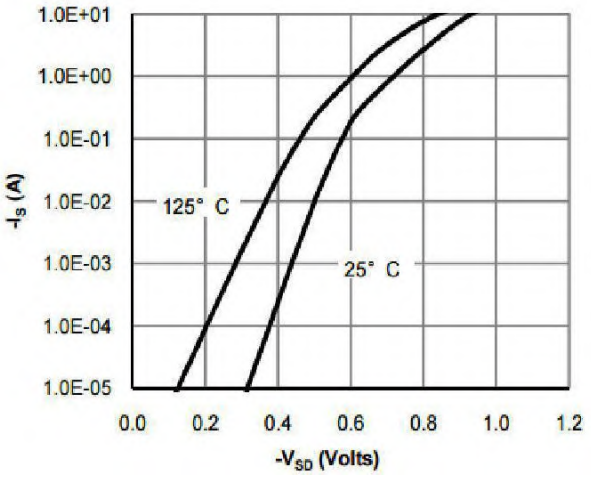


Figure 6: Body-Diode Characteristics (Note D)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

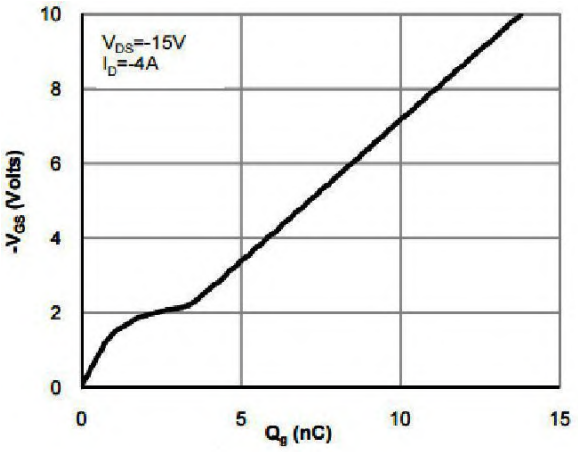


Figure 7: Gate-Charge Characteristics

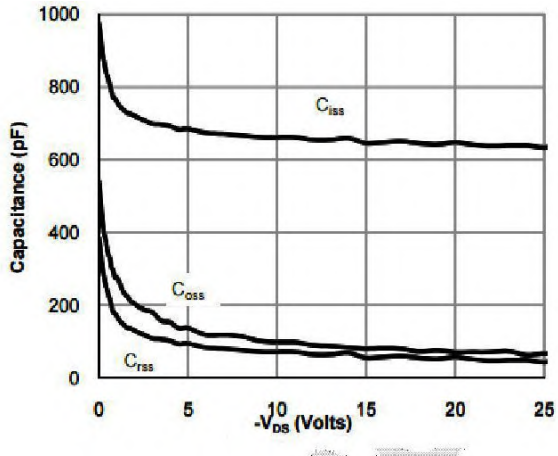


Figure 8: Capacitance Characteristics

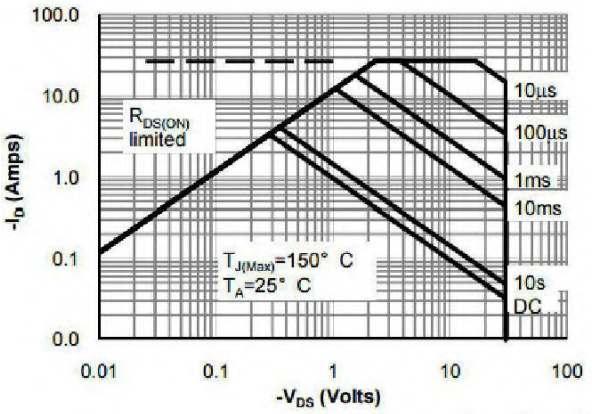


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

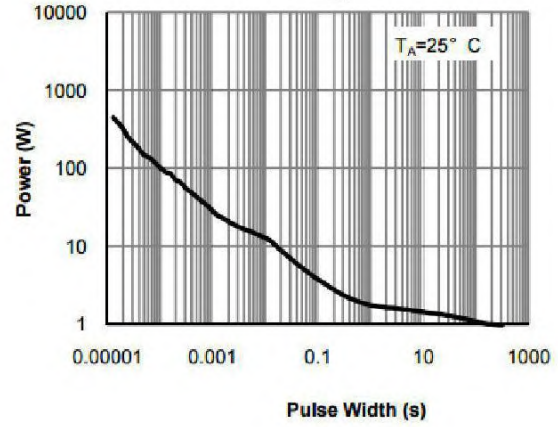


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

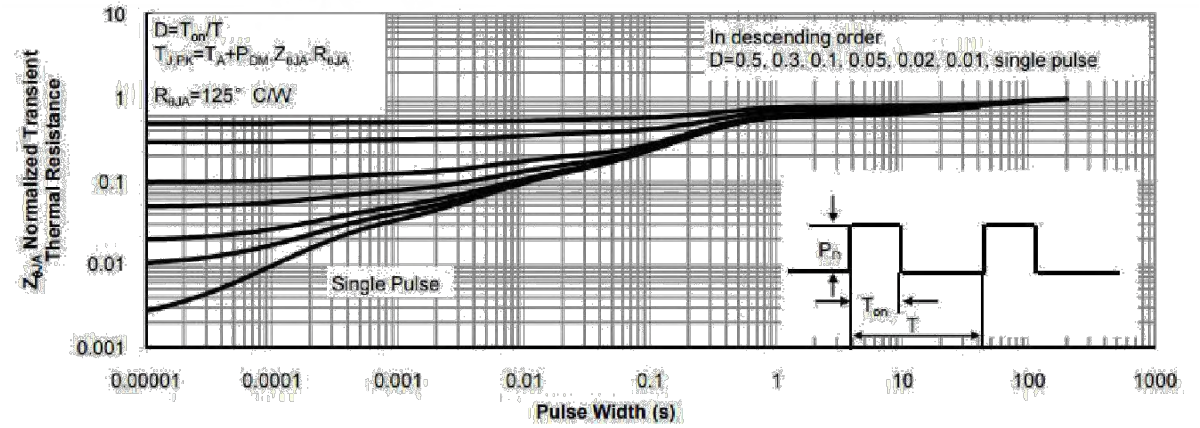
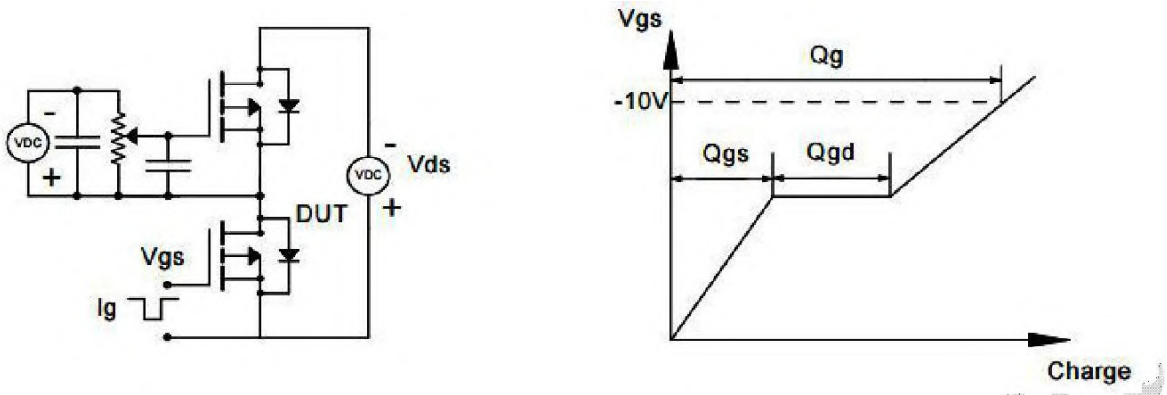
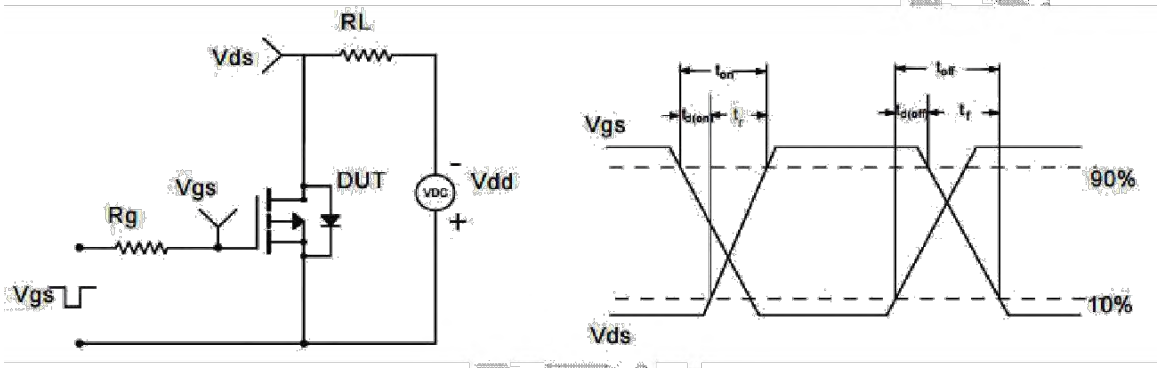


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

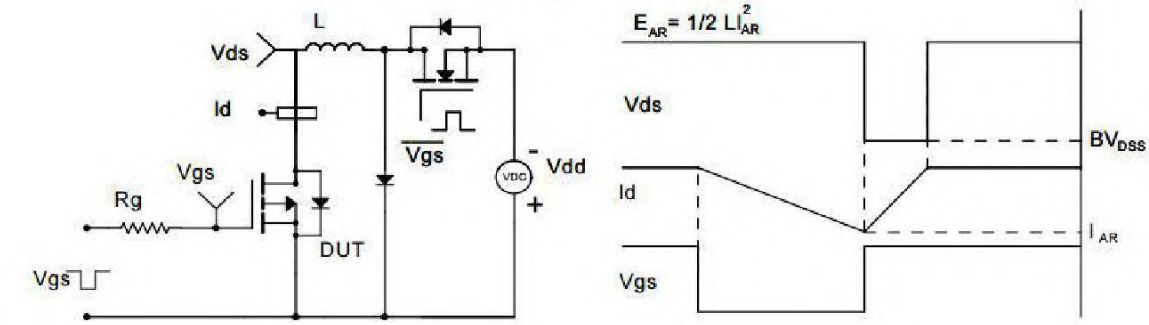
Gate Charge Test Circuit & Waveform



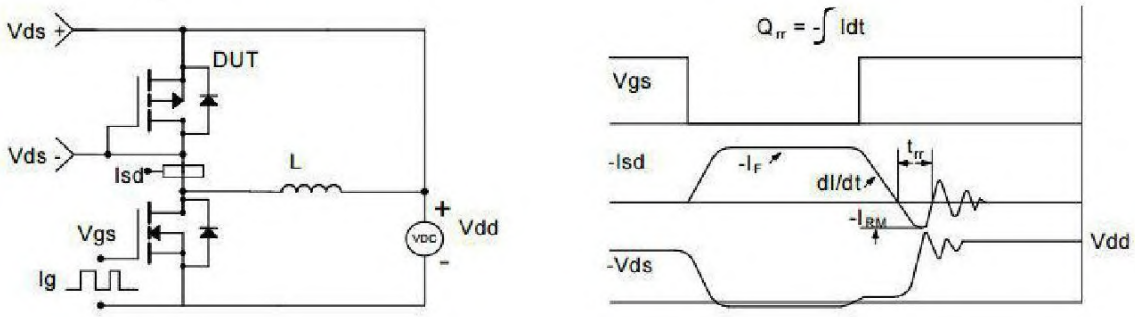
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

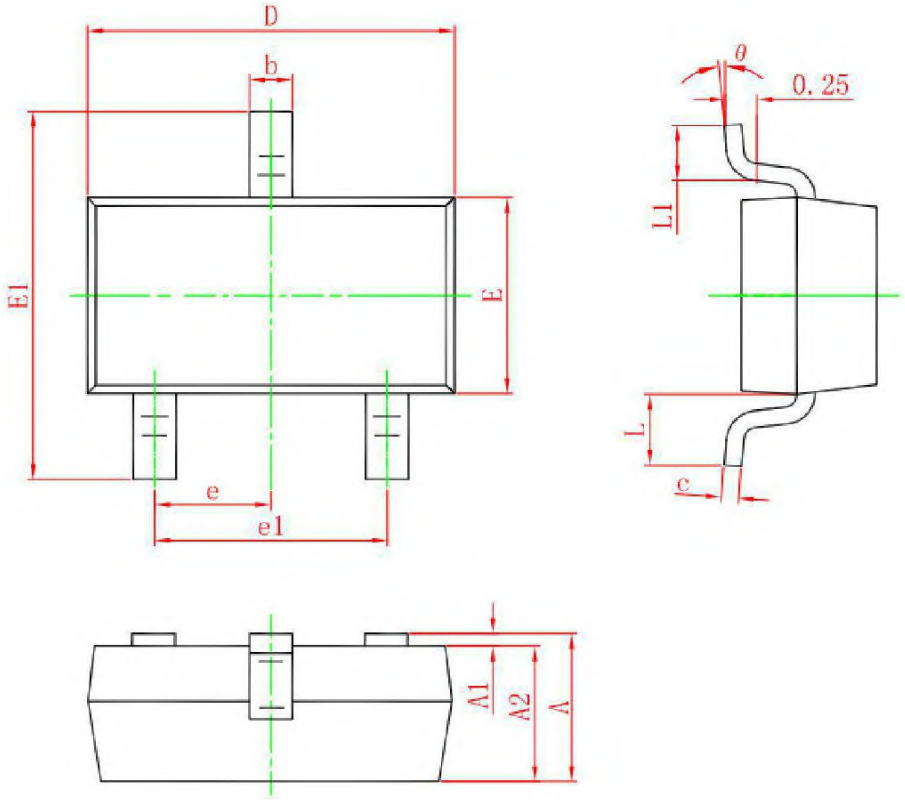


Diode Recovery Test Circuit & Waveforms



Package Information

SOT23-3



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°