GeneralDescription

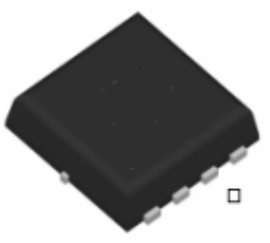
The ZLM0307CE combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

RoHS and Halogen-Free Compliant

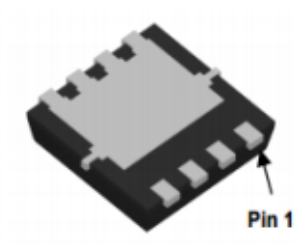
Product Summary

V_{DS}	-30V
I_D(at V_{GS}=-4.5V)	-12A
$R_{DS(ON)}$ (at V_{GS}=-20V)	< 10mΩ
$R_{DS(ON)}$(at V_{GS}=-10V)	<14mΩ
$R_{DS(ON)}$(at V_{GS}=-4.5V)	<20mΩ

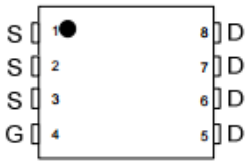
Top View

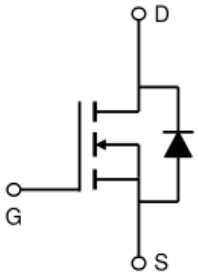


Bottom View



Top View





Absolute MaximumRatings T_A=25℃unless otherwisenoted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
ContinuousDrain Current	T_A=25℃	I_D	-12	A
	T_A=70℃		-10	
PulsedDrainCurrent[C]		I_{DM}	-60	A
Power Dissipation[B]	T_A=25℃	P_D	3.1	W
	T_A=70℃		2	
Storage Temperature Range		T_{STG}	-55 to +150	℃
Operating Junction Temperature Range		T_J	-55 to +150	℃
Thermal Resistance, Junction-to-Ambient [A]		$R_{\theta JA}$	62	℃/W

Electrical Characteristics (TJ=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250uA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V,V_{GS}=0V			-1	uA
I_{GSS}	Gate-Bodyleakagecurrent	V_{DS}=0V,V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250uA	-1		-3	V
$I_{D(ON)}$	Onstate draincurrent	V_{GS}=-4.5V,V_{DS}=-5V	-60			A
$R_{DS(ON)}$	StaticDrain-Source On-Resistance	V_{GS}=-20V,I_D=-12A		5	10	mΩ
		V_{GS}=-10V,I_D=-30A		7	14	mΩ
		V_{GS}=-4.5V,I_D=-15A		14	20	mΩ
g_{FS}	ForwardTransconductance	V_{DS}=-5V,I_D=-10.5A		27		S
V_{SD}	Diode Forward Voltage	I_{DS}=-1A,V_{GS}=0V			-1.2	V
I_S	Maximum Body-Diode ContinuousCurrent				-4	A
DYNAMIC PARAMETERS						
C_{iss}	InputCapacitance	V_{GS}=0V,V_{DS}=-15V, f=1MHz		3500		pF
C_{oss}	OutputCapacitance			510		pF
C_{rss}	Reverse TransferCapacitance			420		pF
SWITCHING PARAMETERS						
Q_g	TotalGate Charge	V_{GS}=-4.5V,V_{DS}=-10V, I_D=-4A		33		nC
Q_{gs}	Gate Source Charge			11		nC
Q_{gd}	Gate Drain Charge			13		nC
$t_{D(on)}$	Turn-OnDelayTime	V_{GS}=-4.5V,V_{DS}=-10V, R_L=2.5Ω,R_{GEN}=3Ω		8		ns
t_r	Turn-On Rise Time			18		ns
$t_{D(off)}$	Turn-OffDelayTime			78		ns
t_f	Turn-OffFallTime			42		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-4A,dI/dt=500A/μs		30	40	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-4A,dI/dt=500A/μs		22		nC

Notes:

A. is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference isdefined as the solder mounting surface of the drain pins.RθJC is guaranteed by design while $R_{\theta CA}$ is determined by theuser's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.

B.The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C.Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initialTJ=25°C.

D.The static characteristics in Figures 1 to 6 are obtained using <300 s pulses, duty cycle 0.5% max.

E.These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

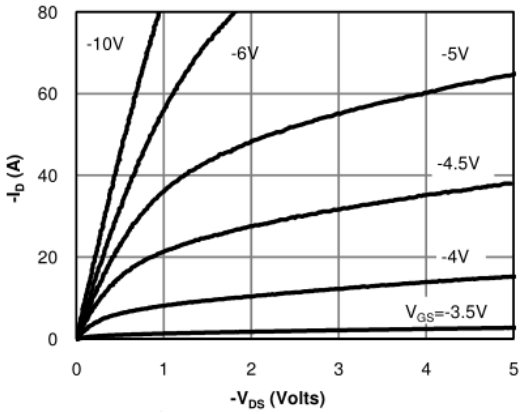


Fig 1: On-Region Characteristics (Note D)

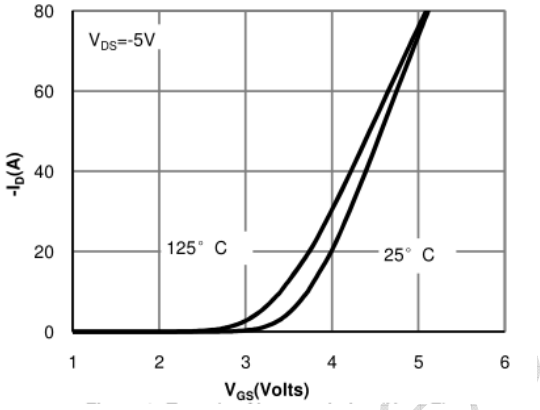


Figure 2: Transfer Characteristics (Note D)

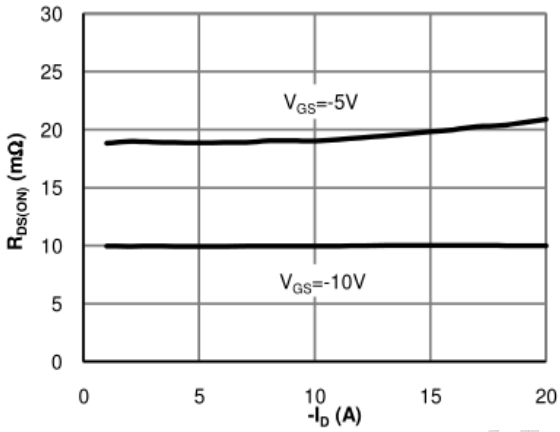


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note D)

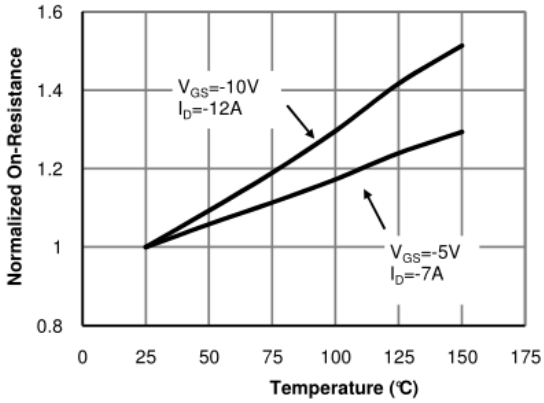


Figure 4: On-Resistance vs. Junction Temperature (Note D)

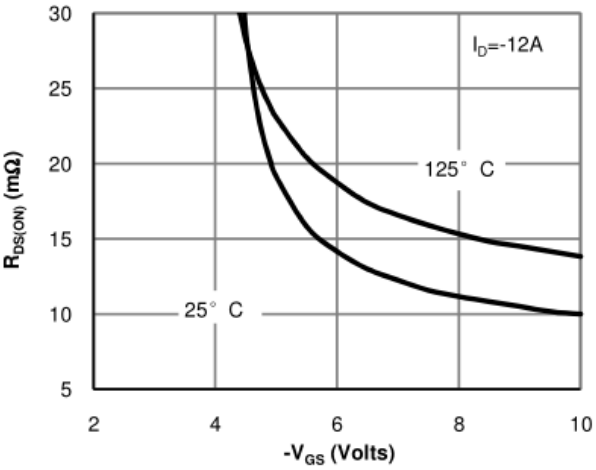


Figure 5: On-Resistance vs. Gate-Source Voltage (Note D)

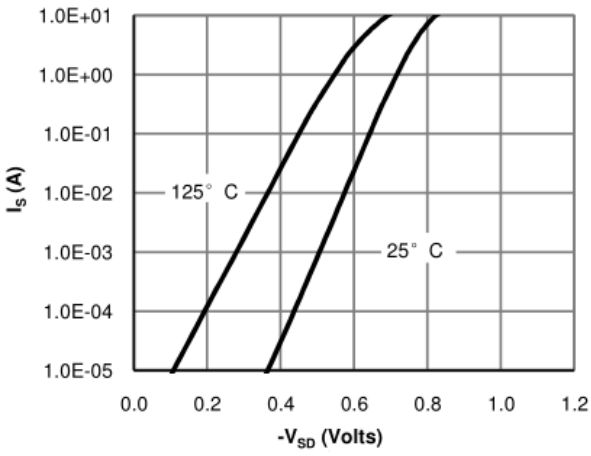


Figure 6: Body-Diode Characteristics (Note D)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

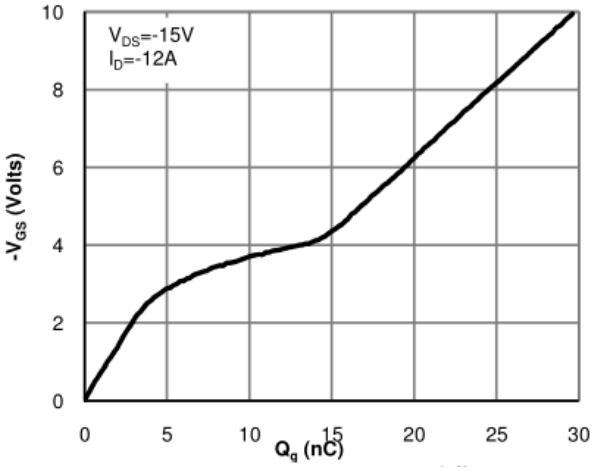


Figure 7: Gate-Charge Characteristics

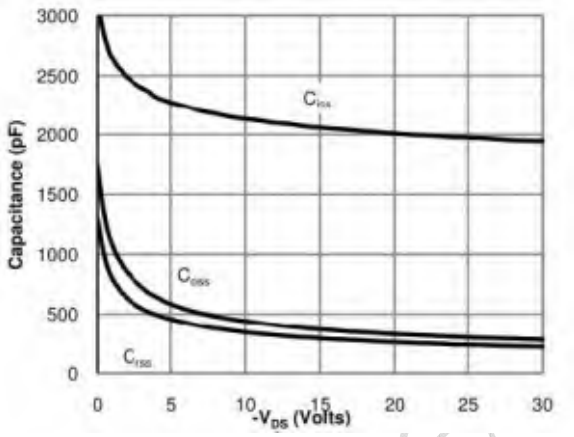


Figure 8: Capacitance Characteristics

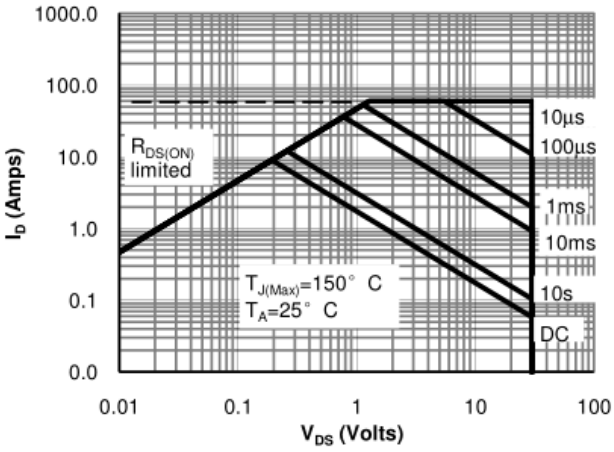


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

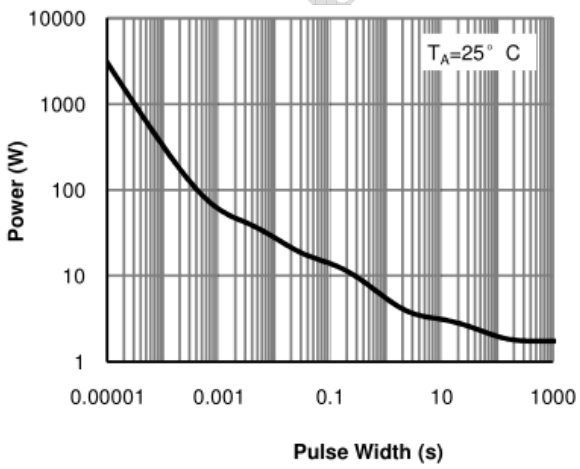


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

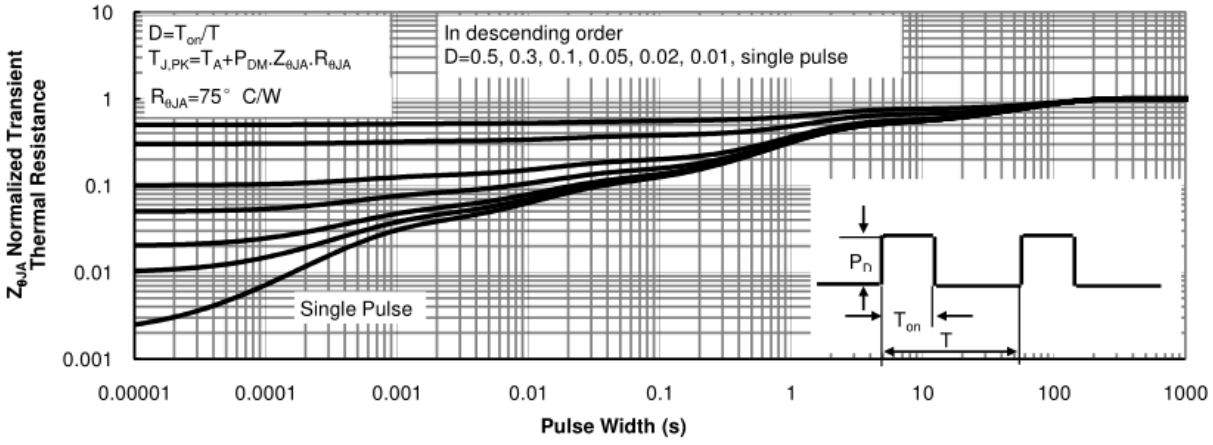
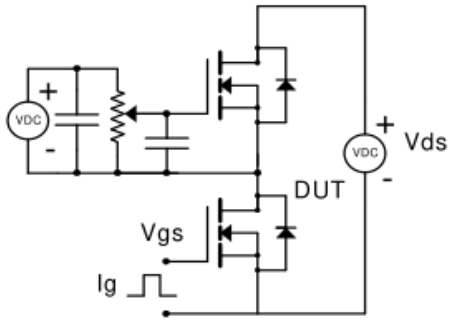
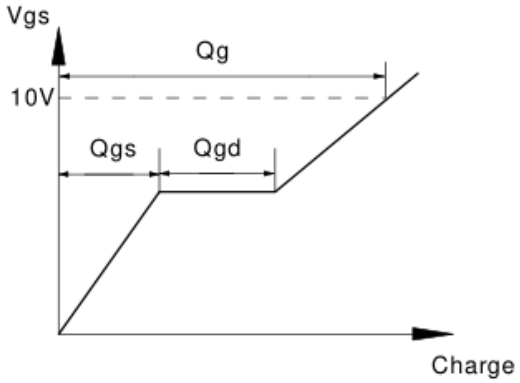


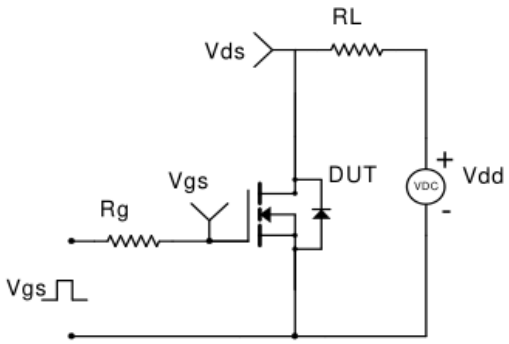
Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

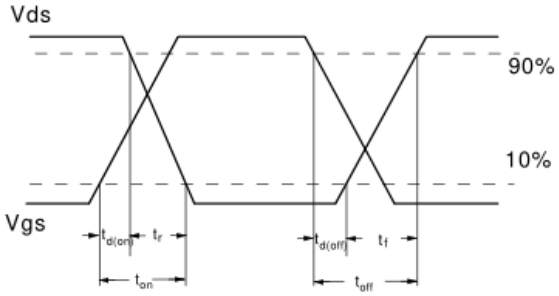
Gate Charge Test Circuit & Waveform



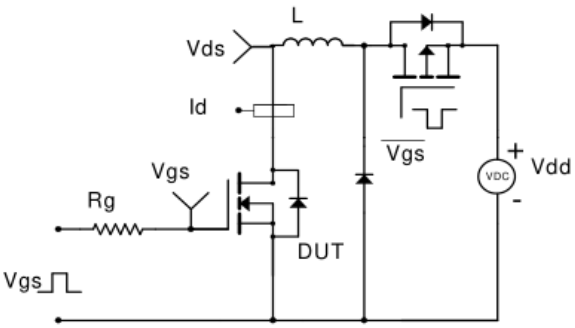


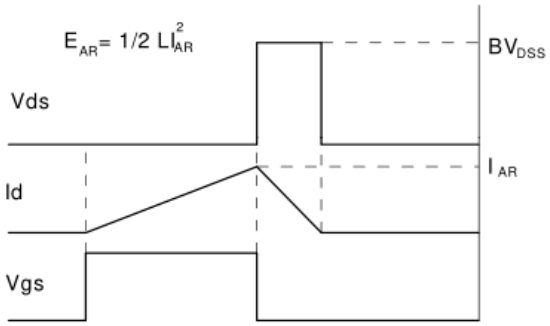
Resistive Switching Test Circuit & Waveforms



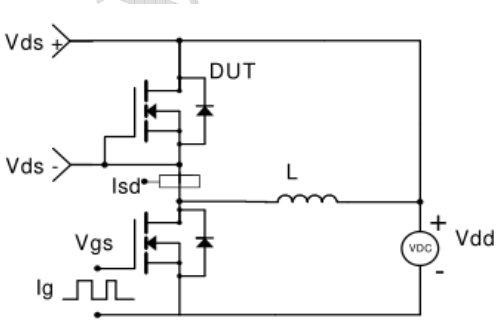


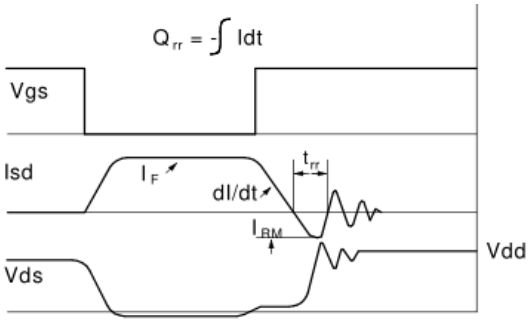
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





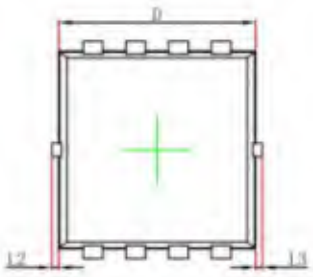
Diode Recovery Test Circuit & Waveforms

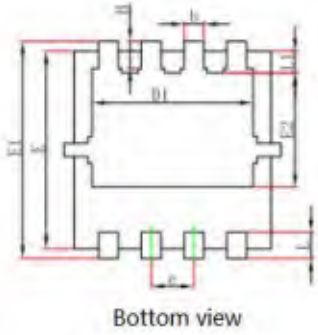


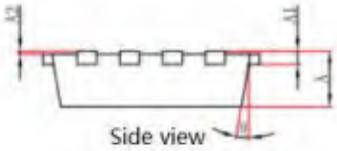


Package Information

PDFN3*3-8L







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°