General Description

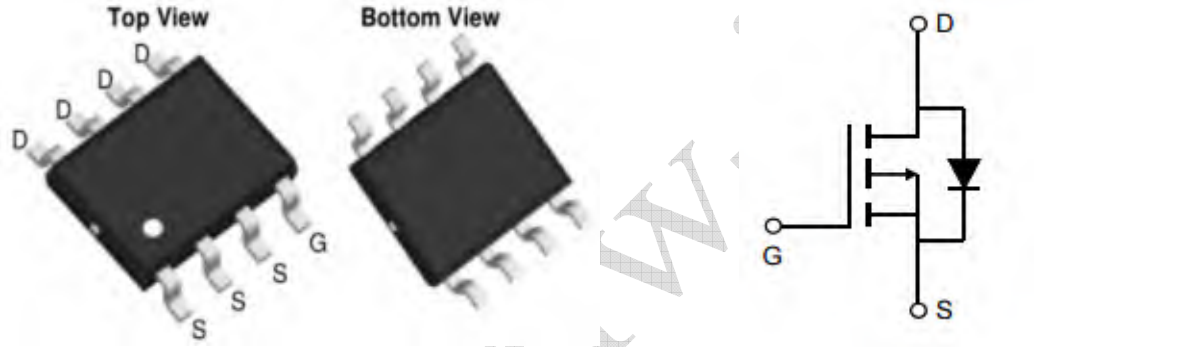
These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

Applications

- Notebook
- Load Switch
- Battery Protection
- Hand-held Instruments
- USB cable

Product Summary

- V_{DS} -30V
- I_D (at V_{GS} =10V) -5.1A
- $R_{DS(ON)}$ (at V_{GS} =-10V) < 32mΩ
- $R_{DS(ON)}$ (at V_{GS} =-4.5V) < 46mΩ



Absolute MaximumRatings （T_A=25℃unless otherwisenoted）

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
ContinuousDrain Current	T_A=25℃	I_D	-5.1	A
	T_A=70℃		-3.2	
PulsedDrainCurrent[A]		I_{DM}	-20	A
Power Dissipation	T_A=25℃	P_D	1.56	W
	T_A=70℃		0.9	
Storage Temperature Range		T_{STG}	-55 to +150	℃
Operating Junction Temperature Range		T_J	-55 to +150	℃
Thermal Resistance, Junction-to-Ambient		$R_{\theta JA}$	80	℃/W

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Electrical Characteristics (TJ=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250uA, V_{GS}=0V	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V,V_{GS}=0V			1	uA
I_{GSS}	Gate-Bodyleakagecurrent	V_{DS}=0V,V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250uA	-1.2	-1.6	-2.2	V
$I_{D(ON)}$	Onstate draincurrent	V_{GS}=10V,V_{DS}=5V	-20			A
$R_{DS(ON)}$	StaticDrain-Source On-Resistance	V_{GS}=-10V,I_D=-4A		27	32	mΩ
		V_{GS}=-4.5V,I_D=-2A		38	46	mΩ
g_{FS}	ForwardTransconductance	V_{DS}=-5V,I_D=-4.1A		9		S
V_{SD}	Diode Forward Voltage	I_{DS}=-1A,V_{GS}=0V		-0.7	-1	V
I_S	Maximum Body-Diode ContinuousCurrent				-5.1	A
DYNAMIC PARAMETERS						
C_{iss}	InputCapacitance	V_{GS}=0V,V_{DS}=-15V, f=1MHz		760	1280	pF
C_{oss}	OutputCapacitance			122	210	pF
C_{rss}	Reverse TransferCapacitance			88	175	pF
SWITCHING PARAMETERS						
Q_g	TotalGate Charge[2,3]	V_{GS}=-4.5V,V_{DS}=-15V, I_D=-5A		8	15	nC
Q_{gs}	Gate Source Charge[2,3]			3.3	6	nC
Q_{gd}	Gate Drain Charge[2,3]			2.3	5	nC
$t_{D(on)}$	Turn-OnDelayTime[2,3]	V_{GS}=-10V,V_{DS}=-15V, R_G=6Ω,I_D=-1A		4.6	9	ns
t_r	Turn-On Rise Time[2,3]			14	26	ns
$t_{D(off)}$	Turn-OffDelayTime[2,3]			34	58	ns
t_f	Turn-OffFallTime[2,3]			18	35	ns

Notes:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%.
3. Essentially independent of operating temperature.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

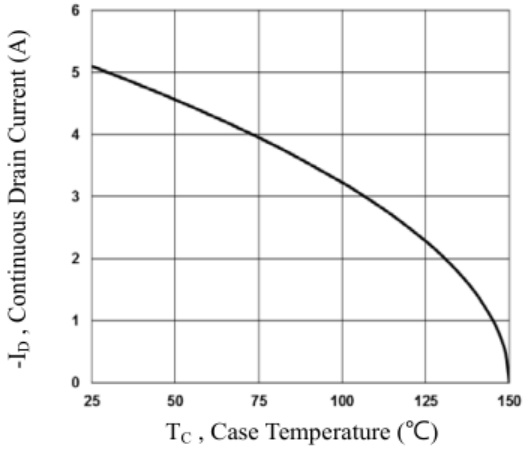

Fig 1: Continuous Drain Current vs. T_C

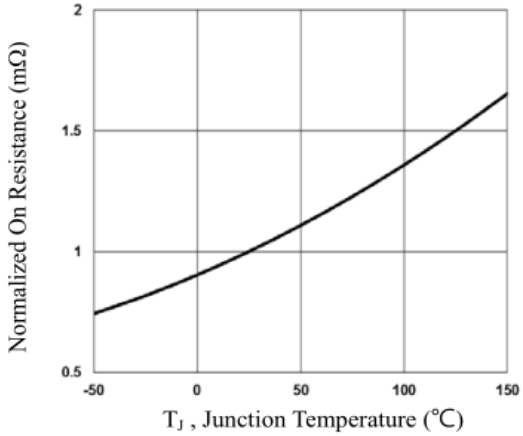

Fig.2 Normalized RDSON vs. T_J

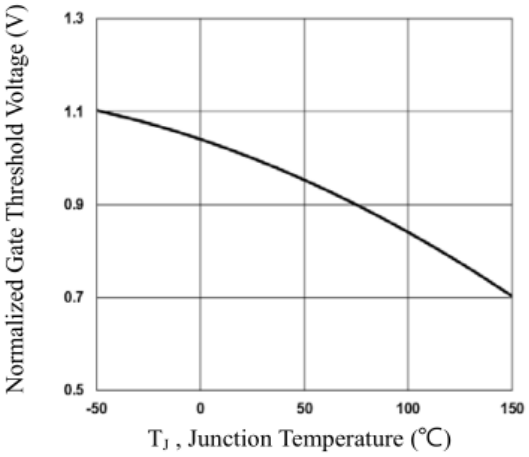

Figure 3: Normalized V_{th} vs. T_J

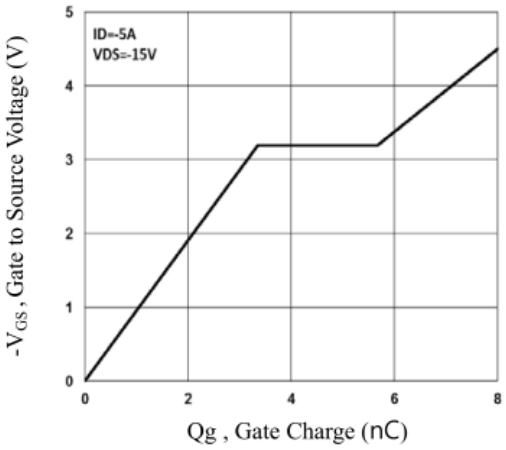

Figure 4: Gate Charge Waveform

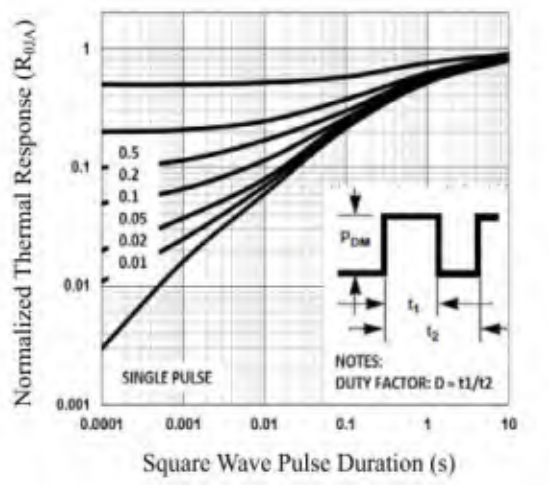

Figure 5: Normalized Transient Impedance

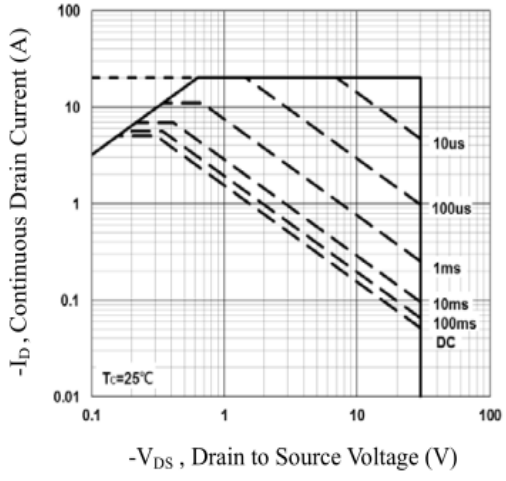

Figure 6: Maximum Safe Operation Area

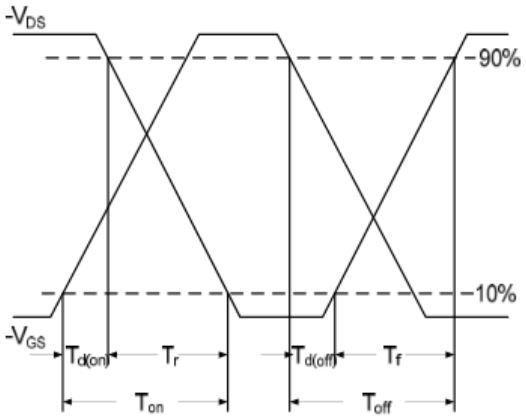

Figure 7: Switching Time Waveform

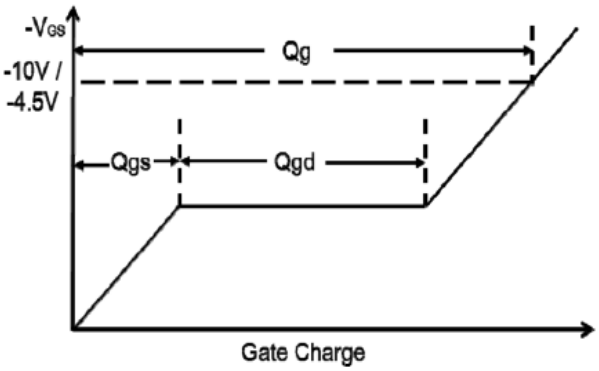

Figure 8: Gate Charge Waveform

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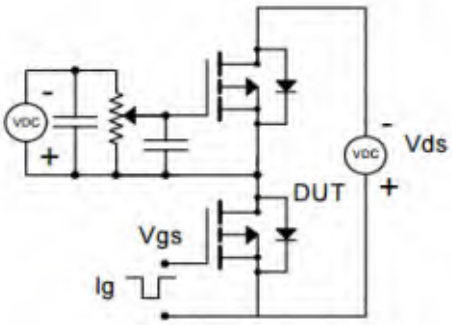
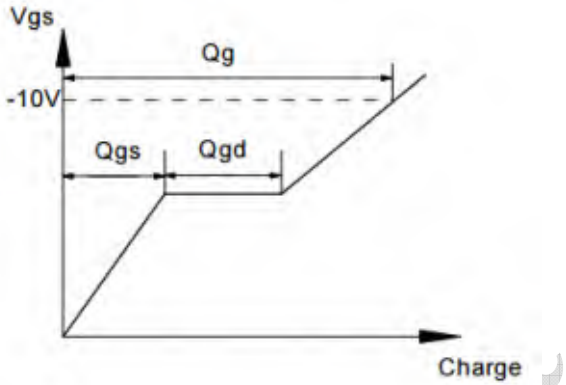
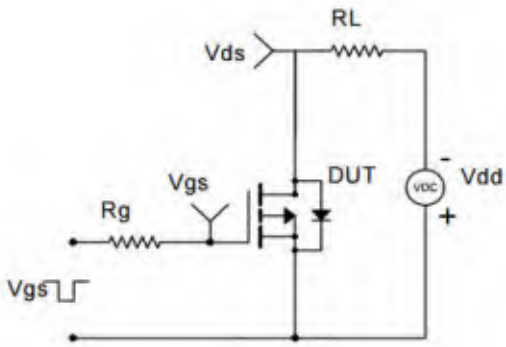
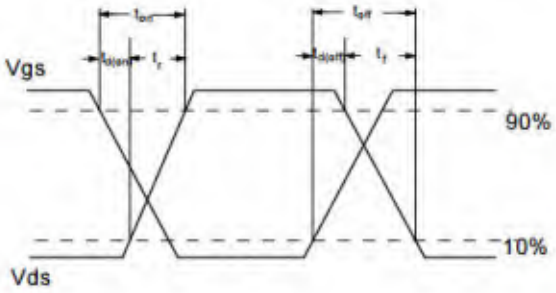
Gate Charge Test Circuit & Waveform



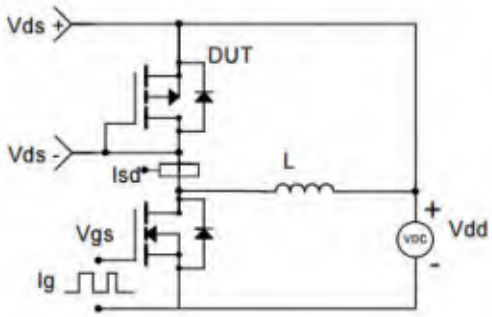


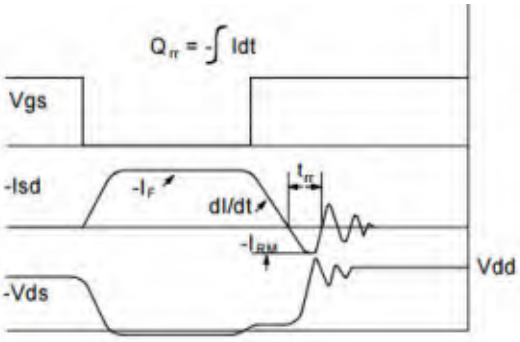
Resistive Switching Test Circuit & Waveforms





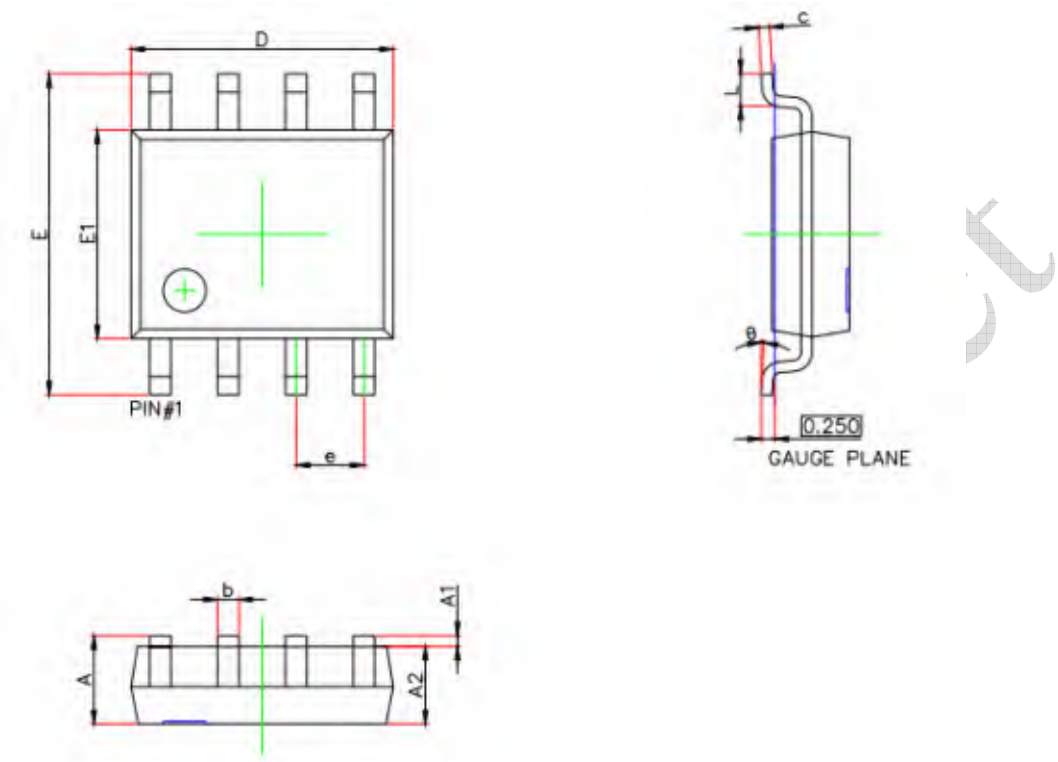
Diode Recovery Test Circuit & Waveforms





Package Information

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 （BSC）		0.050 （BSC）	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°